**Instructions for creating the block diagram in vivado**

**(Updated June 28th, 2024)**

Download and set up [Vivado](https://www.xilinx.com/support/download.html)

Study [this Red Pitaya tutorial](https://antonpotocnik.com/?p=487360) from Anton Potocnik.

Set up the project in Vivado based on his project #4: Frequency counter.

Your block diagram in Vivado will look like this:

A diagram of a computer

Description automatically generated

Delete the Frequency counter block, signal decoder block, and xlc\_reset block.

Input the Verilog code from the [Github repository](https://github.com/RomiGilat/PVMae).

The goal is to modify the block diagram to make it look like this:

**A diagram of a computer

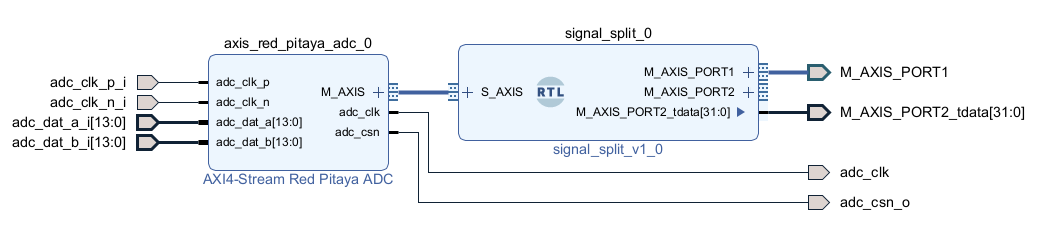
Description automatically generatedGeneral Block Diagram**

Frequency\_counter\_cycles has a value of 2.

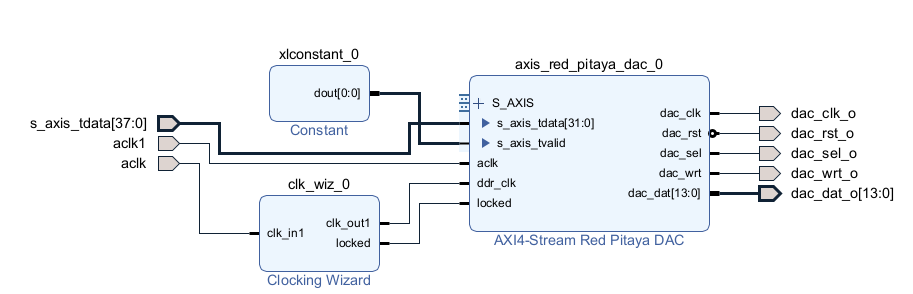
The frequency counter block used in this project is a modified version from the one in the tutorial. The code for this one is in the github repo as well.

The following pictures correspond to the individual blocks that make up the hierarchy blocks (dark blue blocks):

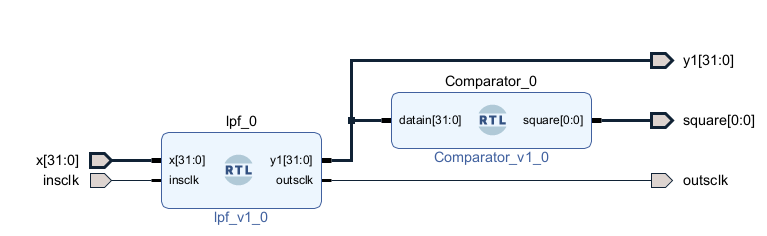
**ADC Block:**

This signal split module is a modified version of the one in the original block from the tutorial. The code for this one is in the github repo as well.

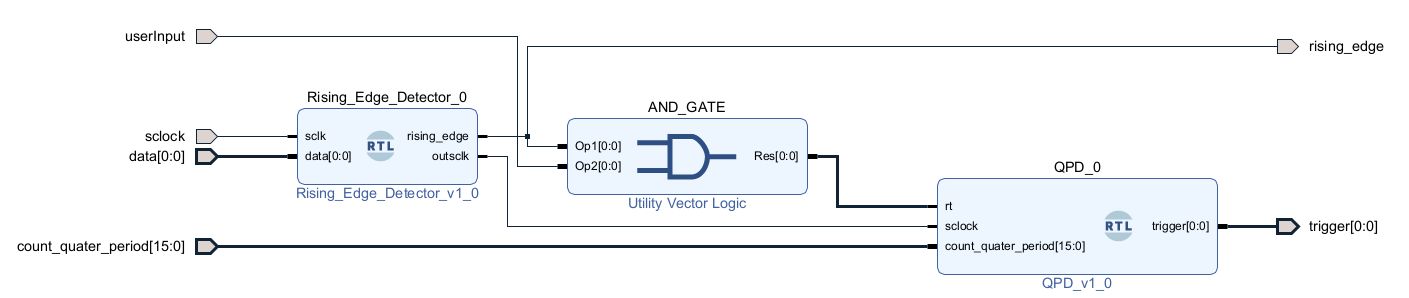
**DAC Block:**



This block is exactly the same as the one in the tutorial.

**DSP Block:** 

**Trigger Block:**



After you are finished setting up the block diagram, generate the bitstream file which you then copy to the RP using WinSCP and execute it by using PuTTy.